

WHAT IS CLAIMED IS:

1           1. An integrated circuit device, the device comprising:  
2           a substrate;  
3           an insulating layer overlying the substrate;  
4           a copper metal layer overlying the insulating layer;  
5           an etch stop layer overlying the copper metal layer;  
6           an interlayer dielectric material overlying the etch stop layer, the interlayer  
7           dielectric material including an upper surface;  
8           a plurality of via openings defined within a region of the interlayer dielectric  
9           layer from the upper surface through the etch stop layer to the copper metal layer;  
10           a copper fill material within each of the plurality of via openings to define a  
11           plurality of copper structure extending from the upper surface through the etch stop layer to  
12           the copper metal layer;  
13           a first barrier metal layer overlying each of the plurality of copper structures to  
14           define a first electrode of a capacitor structure;  
15           an insulating layer overlying the first barrier metal layer to define an insulating  
16           layer for the capacitor structure; and  
17           a second barrier metal layer overlying the insulating layer to define the second  
18           electrode.

1           2. The device claim 1 wherein the insulating layer is silicon nitride and  
2           the etch stop layer is nitride.

1           3. The device of claim 1 wherein the insulating layer has a thickness of  
2           about 200 to about 1000 Angstroms and more preferably 300 to 700 Angstroms.

1           4. The device of claim 1 wherein the insulating layer is PECVD nitride.

1           5. The device of claim 1 wherein the first barrier metal layer and the  
2           second barrier metal layer comprises a tantalum material or a titanium material.

1           6. The device of claim 1 wherein each of the plurality of metal structures  
2           has a width of less than 0.3 microns and a height of greater than about 7000 Angstroms.

1           7. The device of claim 1 wherein the capacitor structure has a capacitance  
2           ranging from about 0.5 to about 5 Femto Farads per square micron.

1                   8.       The device of claim 1 further comprising a metal connector layer  
2       overlying the second barrier metal layer.

1                   9.       The device of claim 1 wherein the plurality of metal structures includes  
2       at least ten or more.

1                   10.      The device of claim 1 wherein the copper layer comprises a second  
2       portion, the second portion defines an interconnect layer.

1                   11.      An integrated circuit device, the device comprising:  
2                   a substrate;  
3                   an insulating layer overlying the substrate;  
4                   a copper metal interconnect layer overlying the insulating layer;  
5                   a capping layer overlying the copper interconnect metal layer to isolate the  
6       copper metal interconnect layer from overlying structures;  
7                   a first barrier metal layer overlying the capping layer, the first barrier metal  
8       layer being free from the copper interconnect layer to define a first electrode structure;  
9                   an insulating layer overlying the first barrier metal layer to define a capacitor  
10      dielectric structure;  
11                  a second barrier metal layer overlying the insulating layer to define a second  
12      electrode structure;  
13                  an etch stop layer overlying the second barrier metal layer;  
14                  an interlayer dielectric material overlying the etch stop layer, the interlayer  
15      dielectric material including an upper surface;  
16                  a plurality of via openings defined within a region of the interlayer dielectric  
17      layer from the upper surface through the etch stop layer to the second barrier metal layer;  
18                  a copper fill material within each of the plurality of via openings to define a  
19      plurality of copper structure extending from the upper surface through the etch stop layer to  
20      the second barrier metal layer; and  
21                  an upper metal layer formed overlying the plurality of copper metal structures.

1                   12.      The device of claim 11 wherein the capping layer and the first barrier  
2       metal layer maintain the capacitor insulating layer free from copper impurities.

1               13.     The device of claim 11 wherein the capping layer maintains the  
2     capacitor-insulating layer free from copper impurities during subsequent processing of the  
3     device.

1               14.     The device of claim 11 wherein the device is a mixed signal device  
2     having a frequency range from about 1 MHz and greater.

1               15.     The device of claim 11 wherein the capping layer PE CVD nitride.

1               16.     The device of claim 11 wherein the capping layer has a thickness of  
2     over 300 Angstroms.

1               17.     A method for manufacturing integrated circuit devices, the method  
2     comprising:

3               providing a substrate;

4               forming an insulating layer overlying the substrate;

5               forming a copper metal interconnect layer overlying the insulating layer;

6               forming a capping layer overlying the copper interconnect metal layer to

7     isolate the copper metal interconnect layer form overlying structures;

8               forming a first barrier metal layer overlying the capping layer, the first barrier  
9     metal layer being free from the copper interconnect layer to define a first electrode structure;

10              forming an insulating layer overlying the first barrier metal layer to define a

11     capacitor dielectric structure;

12              forming a second barrier metal layer overlying the insulating layer to define a  
13     second electrode structure;

14              forming an etch stop layer overlying the second barrier metal layer;

15              forming an interlayer dielectric material overlying the etch stop layer, the  
16     interlayer dielectric material including an upper surface;

17              forming a plurality of via openings defined within a region of the interlayer  
18     dielectric layer from the upper surface through the etch stop layer to the second barrier metal  
19     layer;

20              providing a copper fill material within each of the plurality of via openings to  
21     define a plurality of copper structure extending from the upper surface through the etch stop  
22     layer to the second barrier metal layer; and

23 forming an upper metal layer formed overlying the plurality of copper metal  
24 structures.

1 18. The method of claim 17 further comprising planarizing exposed  
2 portions of the copper fill material.

1 19. The method of claim 17 wherein the upper metal layer comprises  
2 copper material.

1 20. A method for forming an integrated circuit device, the method  
2 comprising:

3 providing a substrate;  
4 forming an insulating layer overlying the substrate;  
5 forming a copper metal layer overlying the insulating layer;  
6 forming an etch stop layer overlying the copper metal layer;  
7 forming an interlayer dielectric material overlying the etch stop layer, the  
8 interlayer dielectric material including an upper surface;

9 forming a plurality of via openings defined within a region of the interlayer  
10 dielectric layer from the upper surface through the etch stop layer to the copper metal layer;  
11 forming a copper fill material within each of the plurality of via openings to  
12 define a plurality of copper structure extending from the upper surface through the etch stop  
13 layer to the copper metal layer;

14 forming a first barrier metal layer overlying each of the plurality of copper  
15 structures to define a first electrode of a capacitor structure;

16 forming an insulating layer overlying the first barrier metal layer to define an  
17 insulating layer for the capacitor structure; and

18 forming a second barrier metal layer overlying the insulating layer to define  
19 the second electrode.